Spread spectrum and PLL technology combine to reduce EMI

Combining state-of-the-art spread spectrum and PLL design offers 10 dB improvement in measured EMI.

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This article will examine the design parameters of a spread spectrum clock generator that uses advanced PLL technology to reduce measured EMI by 10 dB. The result is a design solution to pass tough FCC Class B system qualification.

A numerical model has been successfully developed to implement spread spectrum in Phase-Locked Loops (PLLs). Using this patent pending technology, a modulating signal is generated by circuitry injected into the feedback path of the PLL.

Spread spectrum clock generators are a proven and reliable method to reduce the spectral amplitude of EMI components over a substantial bandwidth. The spread spectrum clock block diagram is shown in Figure 1. This technique includes modulation inside closed loop operation.

By spreading the bandwidth, the amplitude of the synthesized clock signal is decreased with respect to its fundamental and harmonics. As a result of reducing the peak amplitudes, the peak radiated electromagnetic emission level is significantly lower when compared to a typical narrow band signal produced by conventional frequency generators. Spread spectrum clock generation is effective for lowering a signal’s peak power density in spectrum by increasing its bandwidth.

From Figure 1, a time-varying model would be developed by state variable system. Finite difference method is applied to develop the numerical model. Then, the best modulating profile is determined by the least square error method. That range of reference frequency optimizes the solution of modulation shape and silicon area occupied.

**Numerical modeling**

A state variable PLL in time-varying model can be derived as:

\[
\frac{dx}{dt} = A(t) \cdot x(t) + B \cdot u(t)
\]  

The state variable \( x(t) \) is a 3 \( \times \) 1 vector. \( A(t) \) is a 3 \( \times \) 3 time-varying matrix that makes equation (1) be a nonlinear model. \( B \) is simply a constant and \( u(t) \) is a 3 \( \times \) 1 vector. After applying finite difference method to equation (1), the discrete system is defined by equation (2).

\[
x(N+1) = A(N+1) \cdot x(N) + \Delta t(N+1) \\
+ B \cdot u(N) \cdot \Delta t(N+1) + x(N)
\]

\( \Delta t \) is a time step between the present and next cycle. For the given trial values of \( A(N+1) \), \( x(N) \) and \( \Delta t(N+1) \), \( x(N+1) \) can be solved to match any modulation waveform by least square error theory. The equation is iterated until optimal results are received.

**Modulation profile**

The shape of the modulation waveform is critical to maximum EMI reduction. The modulation profile used to accomplish the greatest reduction in EMI is shown in Figure 2. The period of the modulation is shown as a percentage of the period length along the x-axis. The amount that the frequency is varied is shown along the y-axis, also shown as a percentage of the total frequency spread. The modulating signal has a frequency of approximately 31 KHz. Actually, any modulating frequency can be achieved by using feedback path control.

As shown in Figure 3, each harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number, the frequency deviation, the percentage of spread, and the modulation frequency.

**Spread spectrum jitter**

The cycle-to-cycle jitter induced by the modulating clock is insignificant compared to the PLL’s original cycle-to-cycle jitter. For example, applying a 100 MHz clock with \( \pm 1\% \) deviation to Figure 2, the

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**Figure 1. Block Diagram of spread spectrum PLL.**

**Figure 2. Lexmark modulation waveform profile.**
period of the waveform is 50 kHz at 100% location. A 100 MHz clock points to 0% of frequency shift. Then the peak-to-peak period displacement from $f_{min}(-100\%)$ to $f_{max}(+100\%)$ equals $(1/(100\ MHz(1-1\%)))-(1/(100\ MHz(1+1\%))) = 200\ ps$. One half period of modulation takes $10\\mu s$ from $f_{min}$ to $f_{max}$. Thus, the number of clock cycles is $10\ \mu s / 10\ ns = 1000$ in a half modulation period. Therefore, spread spectrum only contributes, on average, $200\ ps / 1000 = 0.2\ ps$ jitter to a 100 MHz clock with $\pm 1\%$ deviation.

**PLL closed loop bandwidth**

The bandwidth of the PLL must be larger than the modulation frequency to allow the modulation signal pass through. Equation 3, a transfer function developed from Figure 1, shows the PLL bandwidth in the frequency domain. VCO is the vco gain of the PLL. CP is the charge pump current and $C_1$, $C_2$, $R_1$ are the components in the loop filter. FBD is the number of feedback divider. $m(t)$ is used for modulating signal.

$$H(s) = \frac{VCO \cdot \frac{\varphi}{C_1} \left( s + \frac{1}{R \cdot C_1} \right)}{s^3 + \frac{C_1 + C_2}{R_1 \cdot C_1 \cdot C_2} \cdot s^2 + \frac{C_1 + \varphi \cdot VCO}{R_1 \cdot C_1 \cdot C_2} + \frac{C_1 \cdot \frac{\varphi \cdot VCO}{FBS} \left( s + \frac{1}{R \cdot C_1 \cdot C_2} \right)}{1 + m(t) \cdot FBS}}$$

Equation 3. The transfer function.

The parameters in Equation 3 are given as $VCO = 50.43\ MHz/v$, $C_1 = 500\ pf$, $C_2 = 2000\ pf$, $R_1 = 5k$, $FBD = 45$ and $\varphi = 1mA$. Figure 4 shows the normalized transfer function in Bode plot form. The -3dB point is located at 100 KHz which is larger than the modulation frequency, but still low enough to prevent high frequency noise from passing through it. The 2 dominant poles can be found at 59.97 KHz using MathCad. Damping factor of PLL is 0.44. After inverse Laplace transform is taken to a unit step times Equation 3, the unit step response presents PLL's acquisition time from one frequency to another frequency.

**Measurement and results**

This feedback path modulation technique has been successfully designed into two product families. In Figure 5, a 50 KHz modulating frequency is used to modulate a 100 MHz clock. The target deviation of the profile is $+0.5\%$. Test results show a 49.78 KHz frequency modulation signal spreading a 100.2785 MHz with peak-peak 0.986 MHz deviation. The measurements show the errors from target profile to be 1.635% maximum in peak-peak deviation and 0.44% maximum in modulation frequency.

Meanwhile the jitter shows only 1 ps increase after turning on the spread spectrum features. Figures 6 shows unmodulated and modulated 100 MHz clock jitter measurements, respectively.

Comparing the modulated and unmodulated fifth harmonic of the clock spectrum measures 8.33 dB reduction in Figure 7.

**Products and applications:**

There are many different families of devices with spread spectrum PLL's incorporated in them. The family upon which this article is based is a single PLL based device which can be provided in 8 or 16 pin SOIC's. Various existing options simply take an input signal with peak-peak 0.986 MHz deviation.

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Figure 3. Clock harmonic with and without SSCG modulation in the frequency domain.

Figure 4. PLL Closed loop bandwidth.

Figure 5. Modulation waveform generated by W48S101 product.
and offer at the output 1 to 6 copies of the input with a selected spread spectrum component added. Some options offer simple multiplication of input frequencies on top of the spread spectrum addition, and through metal mask variations on the base, the device has the ability to provide a wide variety of output frequencies for any given input. A wide variety of systems including printers, fax machines, home video game systems, and disk drives have found spread spectrum clocks useful for some of the frequencies required by their components. Some types of drivers (print heads for example) will not function acceptably using today’s spread spectrum clocks, but future devices are under development as possible solutions for such applications.

A second family of products utilizing spread spectrum technology has two PLLs, but only one of them offers the SSCG feature. This is a line of clock generators for 66 and 100 MHz chip set requirements. Virtually all motherboard manufacturers have embraced the SSCG technology.

Conclusions
The numerical model of spread spectrum control in feedback path is a nonlinear differential system. Finite difference is a very powerful method to solve time-varying nonlinear system solutions. Least square error is a popular numerical method to apply to fit a curve. It always follows the ideal spread spectrum waveform closely. Therefore, the modulation profile is mathematically derived as providing maximized reduction of EMI over a given variation range, without adding any significant amount of cycle-to-cycle clock jitter. All the measured results show good match to target design. Theoretically, feedback modulation is not only able to achieve any deviation precisely, but also to have better EMI reduction. Higher resolution and smooth profile are desired for modulating profile that reduces more power density in all harmonics.

References:

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